The reconfigurable nature of Field Programmable Gate Arrays (FPGAs), together with their relatively low cost and ease of implementation, provided the space industry with an attractive solution for high level computer systems applications. Unfortunately, FPGAs are susceptible to Single Event Effects (SEEs) such as Single Event Transients (SETs), Single Event Upsets (SEUs) and Total ionizing dose effects.

SETs are caused by charged particles depositing charge on circuit elements through ionization. These deposited charges cause elevated local voltage levels in the circuit elements, which leads to incorrect logic values [1].

In a combinational logic element, the charge will leak away (over several hundreds of picoseconds) and the element, and consequently the system, will return to a consistent state. However, when synchronous logic is disturbed by a SET on a clock edge, the temporary incorrect logic value is latched into the register. This incorrect value can then propagate through the rest of the system compromising its functional integrity. SETs that are erroneously latched by a register are called SEUs. High energetic particle strikes to a memory element such as the configuration memory of an FPGA, causing a bit flip, are also called SEUs.

The response of a particular family of FPGAs to SEUs, is a function of its configuration memory [2]. For example, SRAM FPGAs are a family of FPGAs which have configuration memory that consists of SRAM cells. It has been shown that the configuration memory of SRAM based FPGAs is sensitive to SEUs, which causes a bit flip, when struck by an energetically charged particle [2]-[3]. This could cause a change in functionality.

Flash based FPGAs, on the other hand, have configuration memory that consists of Flash memory cells, which have been shown to be resistant to SEUs [4]-[5]. However, previous tests have shown that Flash FPGAs are sensitive to soft errors, or SETs, in the combinational user logic, and to SEUs in the sequential logic elements [6].

In this lecture, we concentrate on the SET mitigation schemes used in FPGAs as well as testing methods to characterize the processors for space applications. In order to use FPGAs in a radiation environment, the mitigation must be applied to the user logic, as well as the memory elements.

A well-known and common mitigation scheme for correcting the SEU errors in FPGAs is Triple Modular Redundancy (TMR) [7]. The main disadvantage of TMR is the excessive area overhead. The hardened design has at least three times more area and power consumption than the original circuit, excluding TMR overhead. When the TMR hardened designs are implemented with a hardware description language or via the manufacturer's software tools, it instantiates redundant triplicate circuits in the user design as well as voting circuits [8]. This method of implementing TMR results in four [9] to seven times [10] resource increase, which limits its usage to reliability-critical applications.

Another common mitigation method, however, to mitigate SETs in the user combinational logic of FPGAs, is to use a SET filter at the inputs of each sequential element [6], [11]-[12]. If SEU hardened latches are used in the circuit's sequential logic, SETs in combinational logic can become the primary source of observable errors, if captured by a memory cell [6], [11]-[12]. To avoid SET capture by any memory element, the SET filter technique could be used [6], [13].

The generally accepted advantage of using the filter technique in FPGAs is to provide a gate count and power savings advantage with respect to TMR. Since SET filters are placed at the inputs of the sequential

elements only, there is no need to provide triple redundancy in the user logic, and it is therefore, assumed that there will be a resource savings with respect to TMR.

The lecture attempts to illustrate the concepts with easy-to-understand general concepts by means of animations.

REFERENCES

[1] P.E. Dodd, L.W. Massengill, "Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics", *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583 – 602, June. 2003.

[2] P. Blain, C. Carmichael, E. Fuller, and M. Caffrey, "SEU mitigation techniques for Virtex FPGA's in space applications", [Online]. Available: http://www.xilinx.com/appnotes/VtxSEU.pdf

[3] Q. Shi and G. K. Maki, "New design techniques for SEU immune circuits," in *9th NASA Symp. VLSI Design*, 2000, pp. 4.2.1–4.2.16.

[4] T. Speers1, J. J. Wang1, B. Cronquist1, J. McCollum1, H. Tseng1, R. Katz2 and I. Kleyner3, "0.25 µm FLASH Memory Based FPGA for Space Applications", Actel Corporation.

[5] J.J. Wang, "Radiation effects in FPGA's", Actel Corporation, 11 May 2004.

[6] S. Rezgui, "New methodologies for SET characterization and mitigation in flash-based FPGAs," IEEE Trans. Nucl. Sci., vol. 54, no. 6, pp. 2512 – 2524, Dec. 2007.

[7] J. von Neumann, "Probabilistic logics and the synthesis of reliable organisms from unreliable components," Automata Studies, no. Ann. Math Studies, no. 34, 1956.

[8] R.L. Shuler, B.L. Bhuma, P.M. O'Neil, J.W. Gambles and S. Rezqui, "Comparison of Dual-Rail and TMR Logic Cost Effectiveness and Suitability for FPGAs with Reconfigurable SEU Tolerance", IEEE Trans. Nucl. Sci, Vol. 56, No.1, pp. 214 – 219, February 2009.

[9] M. Wirthlin, N. Rollins, M. Caffrey, and P. Graham, "Hardness by design techniques for field programmable gate arrays," in Proc. 11th NASA Symp. VLSI Design, May 2003.

[10] K. Morgan, D. McMurtrey, B. Pratt, and M. Wirthlin, "A comparison of TMR with alternative fault-tolerant design techniques for FPGAs," IEEE Trans. Nucl. Sci., vol. 54, no. 6, pp. 2065–2072, Dec. 2007.

[11] A. Balasubramanian, B. L. Bhuva, J. D. Black, and L. W. Massengill, "RHBD techniques for mitigating effects of single-event hits using guard-gates," IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2531–2535, Dec. 2005.

[12] R. L. Shuler, A. Balasubramanian, B. Narasimham, B. L. Bhuva, P. M. O'Neil, and C. Kouba, "The effectiveness of TAG or guard-gates in SET suppression using delay and dual-rail configurations at 0.35 µm," IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3428–3431, Dec. 2006.

[13] S. Rezgui, J. J. Wang, Y. Sun, B. Cronquist, and J. McCollum, "Configuration and Routing Effects on the SET Propagation in Flash-Based FPGAs", IEEE Trans. Nucl. Sci., vol. 55, no. 6, Dec. 2008.

[14] Smith, Farouk. "Overhead and Performance Comparison of SET Fault Tolerant Circuits Used in Flash-based FPGAs." Int. J. Electr. Electron. Eng. Telecommun. (2020).